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Serial No. 09/722,474

Attorney Docket No. 016887/1026

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 27. (Canceled)

28. (Previously presented) A flash memory system comprising:
a memory unit, including a plurality of flash memory cells, for storing data which can be electrically changed;
wherein said flash memory system:
(1) controls said memory unit in order to change the data stored in said memory unit,
(2) detects whether an error has been occurred in read-out data,
(3) counts the number of failure data in changing of data, and
(4) determines that changing of data has been successfully completed if the number of failure data is not larger than a predetermined number, said predetermined number satisfying the condition that the predetermined number of failure data can be corrected.

29. (Canceled)

30. (Previously presented) The flash memory system according to claim 28, wherein a data length of each data stored in said memory unit is one bit.

31. (Previously presented) A flash memory system comprising:
a memory cell unit, including a plurality of flash memory cells, for storing data which can be electrically changed;
wherein said flash memory system:
(1) writes the data and the check code into said memory unit,

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C1 (2) counts the number of errors in the data and the check code after the write, and

(3) issues an alarm if the number has exceeded a predetermined number, said predetermined number satisfying the condition that said predetermined number of errors can be corrected.

32. (Canceled)

4/33. (Previously presented) The flash memory system according to claim 31, wherein a data length of each data stored in said memory unit is one bit.

5/34. (Previously presented) The flash memory system according to claim 28, wherein said flash memory cell is a non-volatile memory transistor, a NAND memory cell is formed from a predetermined number of said non-volatile memory transistors, a source/drain of one transistor of the non-volatile memory transistors being connected to a source/drain of another transistor of the non-volatile memory transistors, the one transistor being adjacent to the another transistor.

6/35. (Previously presented) The flash memory system according to claim 31 wherein said flash memory cell is a non-volatile memory transistor, a NAND memory cell is formed from a predetermined number of said non-volatile memory transistors, a source/drain of one transistor of the non-volatile memory transistors being connected to a source/drain of another transistor of the non-volatile memory transistors, the one transistor being adjacent to the another transistor.

7/36. (Previously presented) An error correction method for a flash memory system, comprising:

programming as a write operation an electrically data changeable memory unit of a plurality of flash memory cells;

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verifying after the programming operation;

C1 ending the programming operation in a case when the result of the verifying is OK, or comparing a programming operations number with a predetermined number in a case when the result of the verifying is No Good (NG);

re-executing the programming operation in a case when the programming operation number is equal to or less than the predetermined number, or in a case when the programming operation number is greater than the predetermined number, counting the number of NG bits to obtain a count number, and comparing the count number with a predetermined count number;

judging that the write operation is OK in a case when the count number is equal to or less than the predetermined count number, and judging that the write operation is No Good (NG) in a case when the count number is greater than the predetermined count number.

37. (Currently Amended) A flash memory system capable of error correction, comprising:

a memory unit, including plurality of flash memory cells, which is configured to store data which can be electrically changed;

a writing circuit, configured to program the memory unit as a write operation and to verify a result of the programming, to end the write operation in a case when the result of the verify is OK, or to compare a program operations number with a predetermined number in a case when the result of the verify is No Good (NG), and to re-execute the programming operation in the case the program operations number is ~~equal to or greater~~ less than the predetermined number;

a verify read circuit configured to execute a verify read operation when the program operations number is equal to the predetermined number;

a judging circuit configured to count a NG-bit number and to compare the NG-bit number with a predetermined count number, and to judge that the write operation is OK in a case when the NG-bit number is equal to or less than the

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predetermined count number, or to judge that the write operation is NG in a case when the NG-bit number is greater than the predetermined number.

9 ~~38~~ (Previously presented) The flash memory system according to claim ~~37~~, wherein said flash memory cell is a non-volatile memory transistor, a NAND memory cell is formed from a predetermined number of said non-volatile memory transistors, a source/drain of one transistor of the non-volatile memory transistors being connected to a source/drain of another transistor of the non-volatile memory transistors, the one transistor being adjacent to the another transistor.
